REMARKS

Claims 3, 13, 14, 17, 28, 29, and 33 have been cancelled without prejudice, and claims 1, 4, 5, 7, 9, 12, 15, 16, 18-21, 32, 35, and 38 have been amended. In addition, the original set of claims filed with the application inadvertently included two claims numbered 36. The second of those claims has been renumbered as claim 37, and former claim 37 has been renumbered as claim 38. Claims 1, 2, 4-12, 15, 16, 18-27, 30-32, and 34-38 are now pending in the application. Applicant respectfully requests reexamination and reconsideration of the application in light of the amendments and the following remarks.

All claims were rejected under 35 USC § 103(b) as obvious in view of US Patent No. 5,652524 to Jennion et al. ("Jennion") in combination with US Patent No. 5,822,166 to Massie ("Massie"), and with respect to some claims, US Patent No. 5,386,189 to Nishimura et al. ("Nishimura"). Applicants respectfully traverse these rejections.

Independent claim 1 describes a method for use in a semiconductor test system in which a temporary change in current drawn at a power terminal of a semiconductor device being tested is sensed and a supplemental current is provided to the power terminal to compensate for the temporary change. Independent claims 16 and 32 describe apparatuses with generally similar features.

In rejecting the independent claims, the PTO relied on a combination of Jennion and Massie. Even if, however, one picks and chooses selected teachings from Jennion and Massie and combines them as the PTO has done, the combination fails to teach or suggest the subject matter of the independent claims of the instant application.

In rejecting the independent claims, the PTO stated that Jennion's programmable power supply 108 provides power to the power input terminal 128 of DUT 104. The PTO further stated that Jennion's V4 122 supplies supplemental current to the power input terminal 128. A close look at Jennion, however, reveals that Jennion's V4 122 is switched into connection with power input terminal 128 in replacement of Jennion's programmable power supply 108. (See Jennion col. 4, lines 17-22.) That is, only one of programmable power supply 108 or V4 122 is connected to power input terminal 128 at any one time. Thus, V4 does not provide "supplemental current" to the power input terminal as required by the independent claims of the instant application. V4 either provides all of the current or none of the current. (See Jennion col. 4, lines 17-22.) Therefore, even if the teachings of Jennion and Massie (and Nishimura for that

matter) are combined as suggested by the PTO, the combination fails to teach or suggest all the features of the independent claims.

Massie does not make up for this deficiency in Jennion. Moreover, there is no motivation—and indeed, it would make no sense—to modify Jennion's V4 122 to provide supplemental current to DUT 104 to compensate for current changes at the power terminal 104. In fact, this would contradict the teachings of Jennion and the express purpose of V4 122, which is to provide a low current power supply for measuring quiescent, that is, static, current drawn by the DUT 104. (See Jennion col. 2, lines 55-63; and col. 3, lines 32-35.)

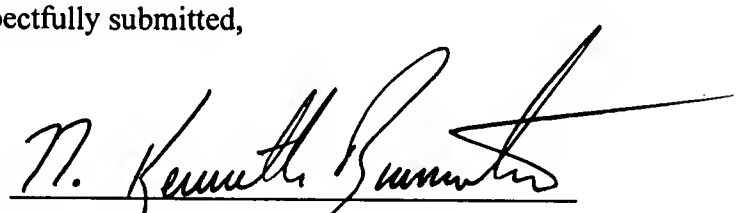
For all of the foregoing reasons, the independent claims (and their dependent claims) patentably distinguish over Jennion, Massie, and Nishimura, whether taken singly or in combination.

In view of the discussion above, Applicants respectfully assert that the application is in condition for allowance. If the Examiner believes that a discussion with Applicants' attorney would be helpful, the Examiner is invited to contact the undersigned at (925) 456-3915.

Although Applicants believe that no extension of time is needed and no fees are due, Applicants petition the Director for any extension of time deemed necessary for acceptance of this paper, and Applicants authorize the Director to charge any fee deemed necessary for acceptance of this paper to Deposit Account No. 50-0285 (order no. P104-US).

Respectfully submitted,

Date: January 29, 2003

By: 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Claims 1, 4, 5, 7, 9, 12, 15, 16, 18-21, 32, 35, and 38 have been amended as follows:

1. (Amended) For use in a semiconductor test system [comprising a probe card and a supplemental current source], a method for reducing variation in a voltage supplied to a power input terminal of a semiconductor device under test, said method comprising:

providing power through [said] a probe card to said power input terminal of said semiconductor device under test;

sensing a temporary change in current drawn by said input terminal of said semiconductor device;

[providing an input signal to said supplemental current source, said input signal corresponding to a temporary change in current drawn by said input terminal of said semiconductor device;] and

providing supplemental current to said input terminal [from said supplemental current source] in response to said [input signal] temporary change in current, said supplemental current compensating for said temporary change in current.

4. (Amended) The method of claim [3] 1, wherein said sensing a temporary change[s] in current drawn by said input terminal comprises sensing a change in current through a bypass capacitor in electrical communication with said power input terminal.

5. (Amended) The method of claim [3] 1, wherein said sensing a temporary change[s] in current drawn by said input terminal comprises sensing a change in current through a conductive path on said probe card that is in electrical communication with said power input terminal.

7. (Amended) The method of claim 1, wherein said supplemental current [source comprises] is provided from an amplifier.

9. (Amended) The method of claim 1, wherein said supplemental current is provided by a supplemental current source [is] disposed on said probe card.

12. (Amended) The method of claim 11, wherein said supplemental current is provided by a supplemental current source [is] disposed on said probe head.

15. (Amended) The method of claim 1[, wherein] further comprising:

[said providing power further comprises] providing power through said probe card to a power input terminal of each of a plurality of [said] semiconductor devices under test;

[said providing an input signal to said supplemental current source further comprises providing an input signal to each of a plurality of supplemental current sources, each said input signal corresponding to current drawn by an input terminal of one of said semiconductor devices;]

sensing a temporary change in current drawn by each said input terminals of each of said semiconductor devices; and

[said providing supplemental current further comprises] providing supplemental current to each of said input terminals [from each of said supplemental current sources] in response to said [input signals each said input signal corresponding to current drawn by an input terminal of one of said semiconductor devices] temporary changes in current, said supplemental current provided to each input terminals compensating for said temporary change in current drawn by said input terminal.

16. (Amended) An apparatus for testing a semiconductor device comprising a power input terminal and signal terminals, said apparatus comprising:

a probe card comprising conductive connection structures for contacting said power input terminal and said signal terminals;

a current sensing device disposed to sense a temporary change in current drawn by said power input terminal; and

a supplemental current source having an output electrically connected to said connection structure for contacting said power input terminal, an input of said supplemental current source electrically connected to a signal corresponding to [a] said temporary change in current drawn by said power input terminal, [caused by a change in a signal on one of said signal terminals, wherein said supplemental current source provides supplemental current to said power input terminal in response to a change in current drawn by said power input terminal] said supplemental current compensating for said temporary change in current.

18. (Amended) The apparatus of claim [17] 16, wherein said current sensing device comprises a current sense coupler.

19. (Amended) The apparatus of claim [17] 16, wherein said current sensing device comprises a current transformer.

20. (Amended) The apparatus of claim [17] 16, wherein said current sensing device is disposed to sense a change in current through a bypass capacitor in electrical communication with said power input terminal.

21. (Amended) The apparatus of claim [17] 16, wherein said current sensing device is disposed to sense a[n] change in current through a conductive path on said probe card that is in electrical communication with said power input terminal.

32. (Amended) An apparatus for testing a semiconductor device comprising a power input terminal and signal terminals, said apparatus comprising:

probe means for providing power to said input terminal and signals to at least one of said signal terminals;

current sensing means for sensing a temporary change in current drawn by said power input terminal; and

supplemental current means for providing supplemental current to said power input terminal in response to [a] said temporary change in current drawn by said power input terminal, [caused by a change in a signal on one of said signal terminals, said supplemental current means having an input and an output, said input electrically connected to a signal that corresponds to said change in current drawn by said power input terminal, said output electrically connected to said power input terminal] said supplemental current compensating for said temporary change in current.

35. (Amended) The apparatus of claim 32, wherein [said] an output of said supplemental current means is electrically connected to said power input terminal through a capacitor.

38 (originally numbered 37). (Amended) The apparatus of claim [36] 37, wherein said probe means provides power to input terminals of each of said plurality of semiconductor devices.